

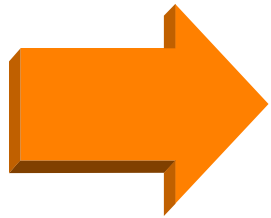
# ***AN INTRODUCTION TO INTEGRATED CIRCUIT TECHNOLOGY AND COSTING***

**The 32nd Annual DoD Cost Symposium  
Feb, 1999**

**Mike Janiga  
MITRE Corporation  
1820 Dolley Madison Blvd  
McLean, Virginia 22102-3481  
(703) 883-7463  
mjaniga@mitre.org**

**MITRE**

# Detailed Cost Estimates



**General Background**

**IC Technology**

**IC Cost Estimation**

**Sources of Information**

# Q. When would you estimate at the IC level?

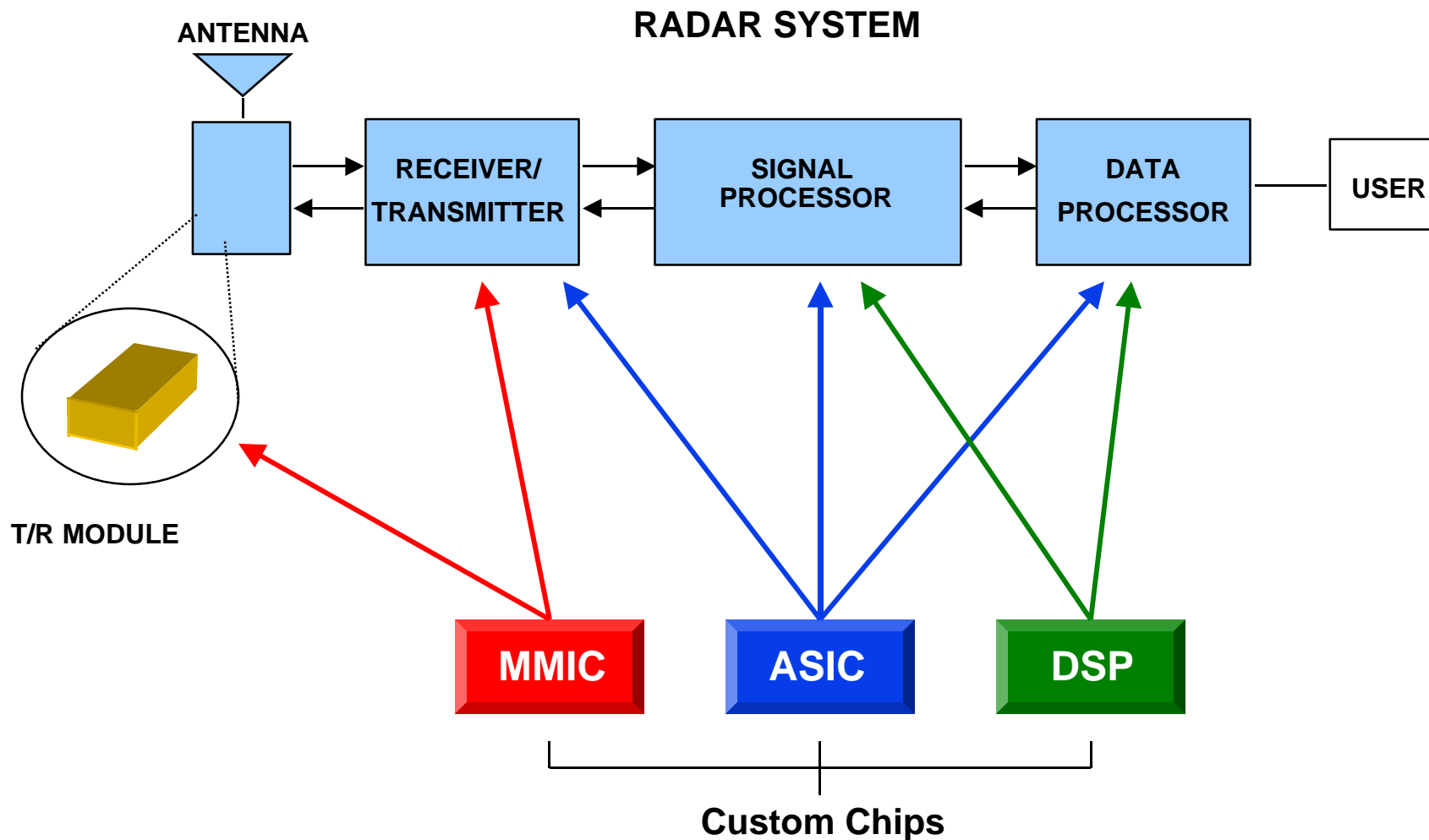


Background

IC Technology

IC Costing

Information



# Moore's Law predicts the future of IC performance

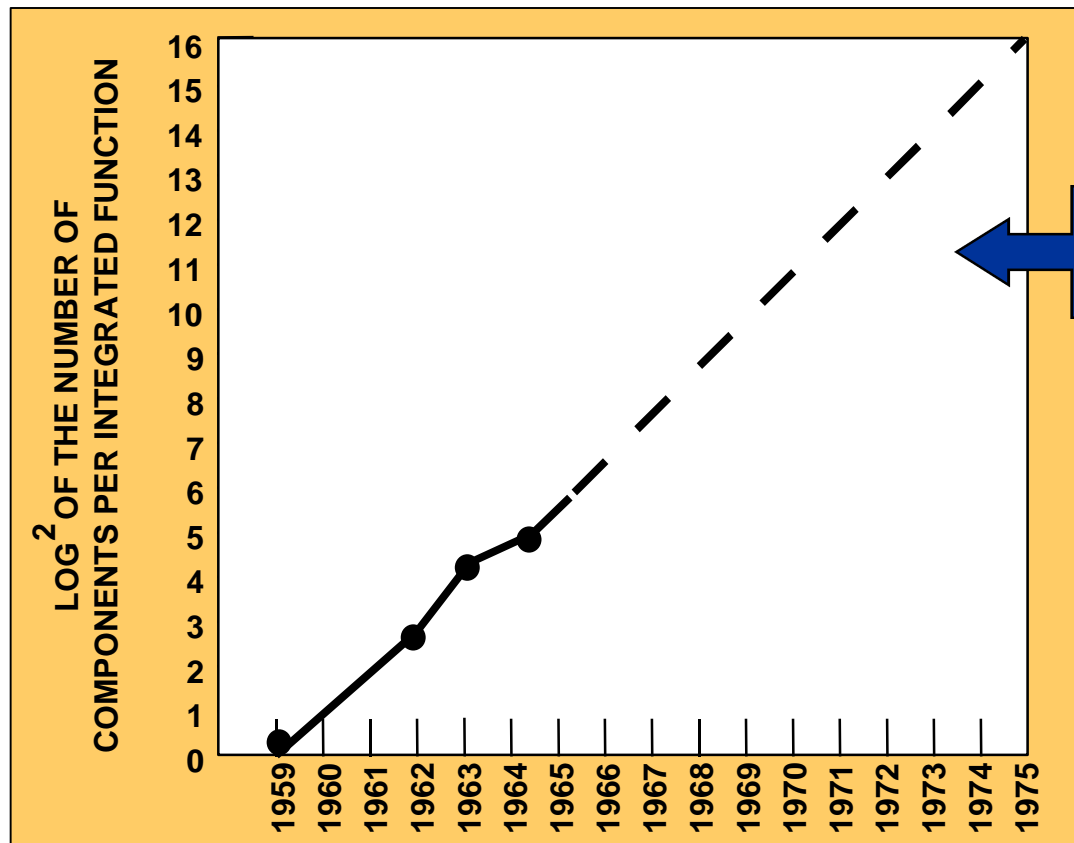
 Background

IC Technology

IC Costing

Information

**Moore's Law** - Chip power doubles every 18 -24 months, while unit cost remains the same.



The Original Moore's Law Plot,  
Electronics, April 1965

# Semiconductor Facts



Background

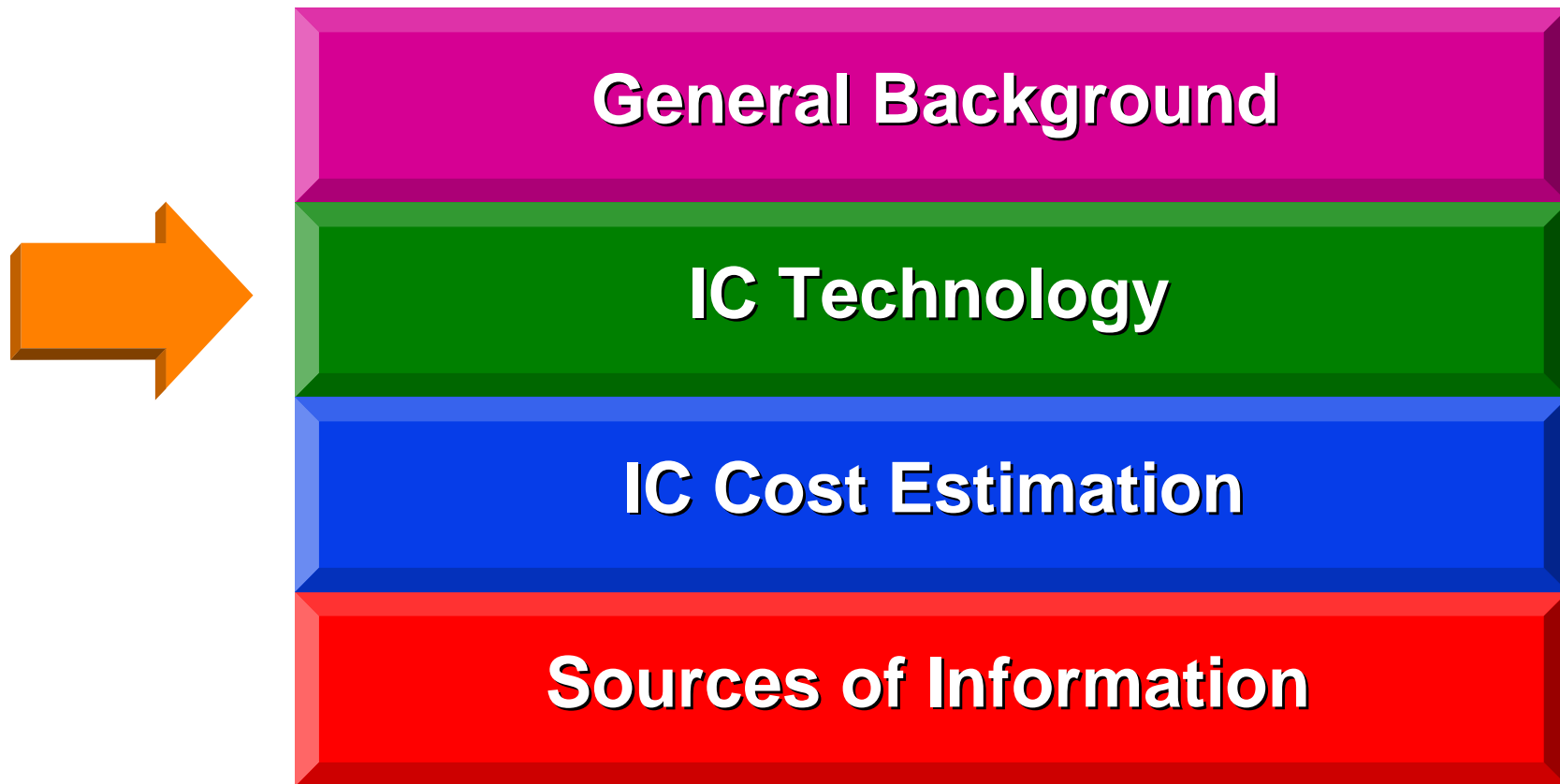
IC Technology

IC Costing

Information

- o **There are approximately 400 IC companies worldwide**
- o **Semiconductors is a \$165B industry**
- o **The DoD has little influence over the semiconductor market**
  - **In 1975, the DoD accounted for 17% of industry sales.**
  - **In 1985, the DoD accounted for 9% of industry sales.**
  - **By 1995, the DoD share dropped to less than 1% of sales.**
- o **In 1998, more than 500 million transistors were manufactured every second.**
- o **If an average cell phone were made with vacuum tubes instead of ICs, it would have to be larger than the Washington Monument.**

# Detailed Cost Estimates



# IC types and their uses



Background

IC Technology

IC Costing

Information

- **Microprocessor** - Performs general control, logic and arithmetic functions.
- **Memory** - stores information or data.
- **Digital Signal Processing (DSP)** - Performs specific arithmetic algorithms.
- **Field Programmable Gate Array (FPGA)** - In field programmable, meaning it can change functionality in real time.
- **Application Specific Integrated Circuit (ASIC)** - Performs customized arithmetic algorithms.
- **Microwave Monolithic Integrated Circuit (MMIC)** - Operates with RF or Microwave energy.

# Degree of IC Specialization

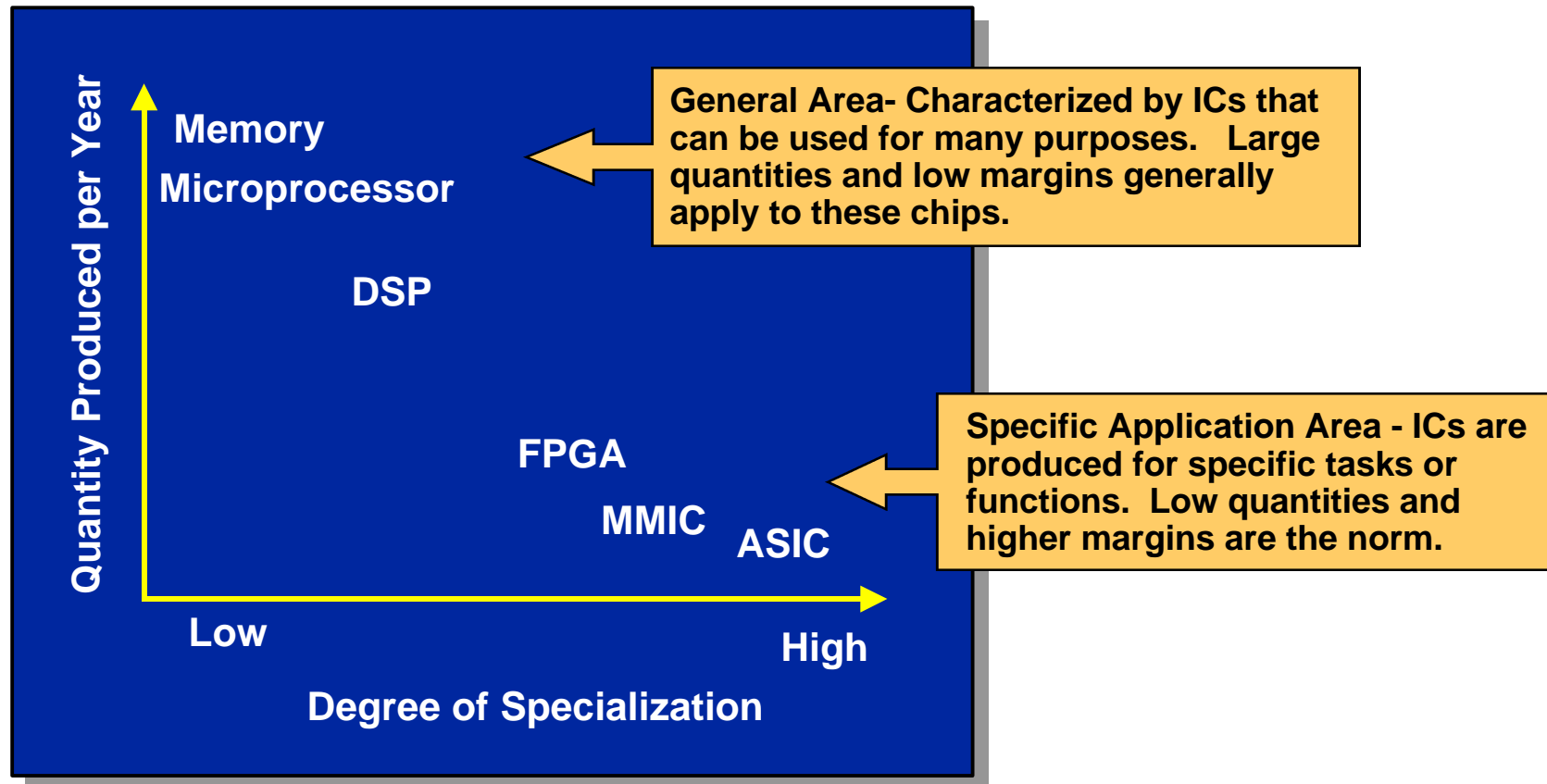


Background

IC Technology

IC Costing

Information



# Smaller feature sizes is key to improved IC performance

Background

IC Technology

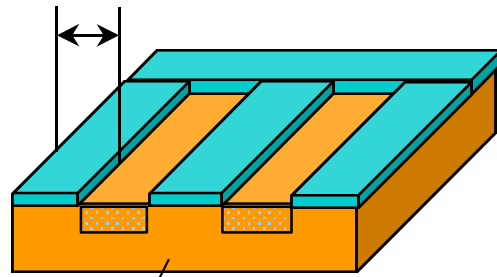
IC Costing

Information

**Feature Size** - The smallest line width or spacing between lines on a chip.

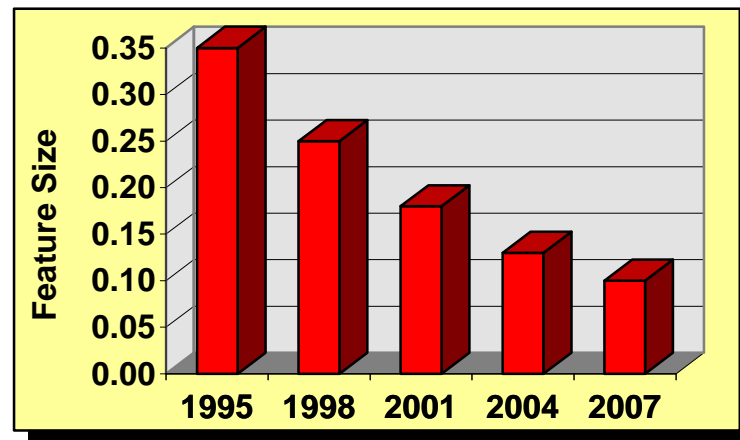
## IC Cross Section

line width =  $0.25\ \mu\text{m}$



Silicon Base

Features such as gates or lines on an IC are so small that they are normally measured in microns.

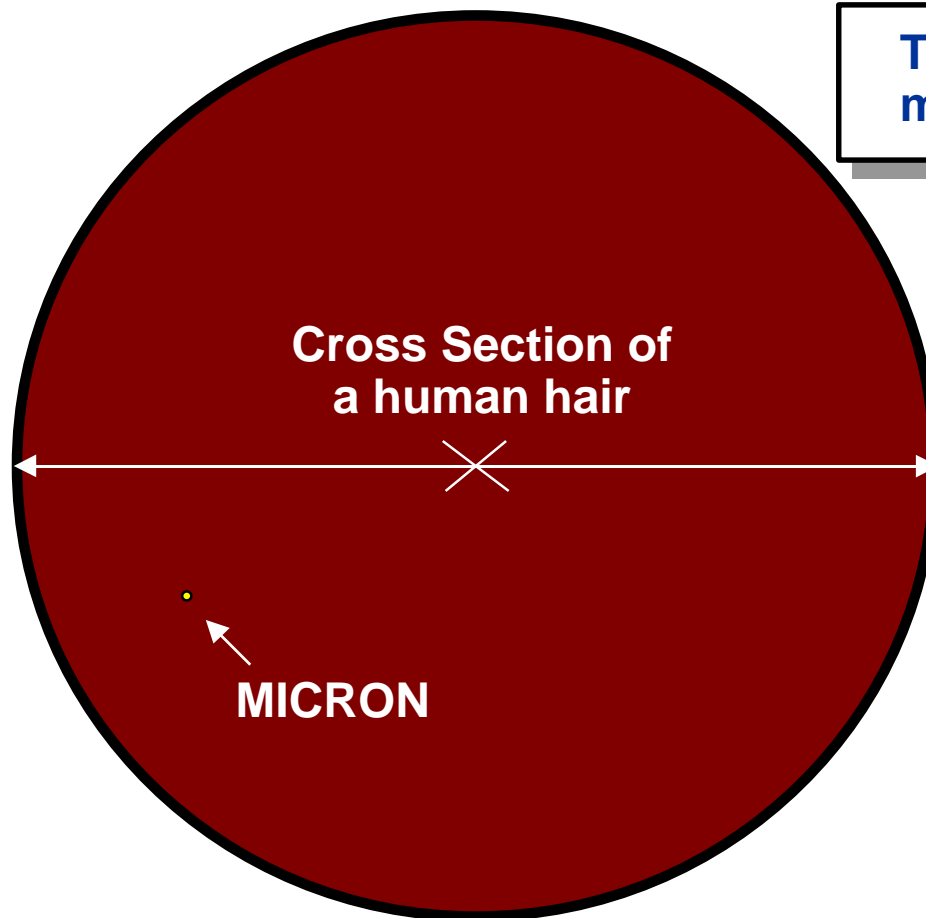


Source: Semiconductor Industry Association

# Relative Size of a Micron

[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

The average human hair is 100 microns in diameter.



## Conversion Table

Unit	Micron
1 Inch	25,400
1 mil	25.4
1 cm	10,000
1 mm	1,000

Source: Van Zant, Microchip Fabrication, 1990.

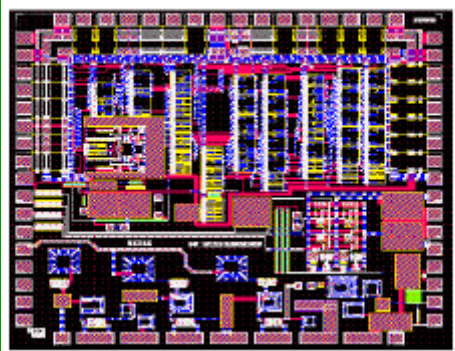
# Major steps in chip fabrication

Background

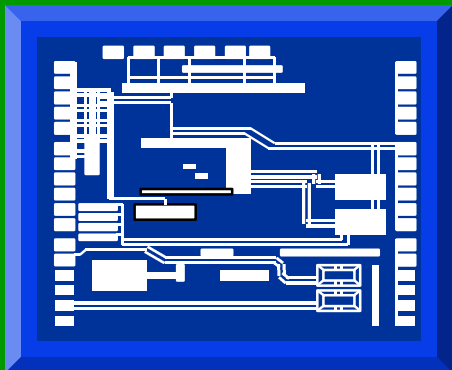
IC Technology

IC Costing

Information

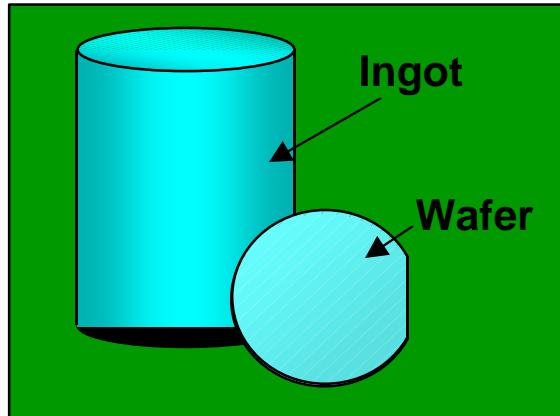


**Step 1** - A detailed design of the IC is created.



**Step 2** - Masks are made of each layer of the IC.

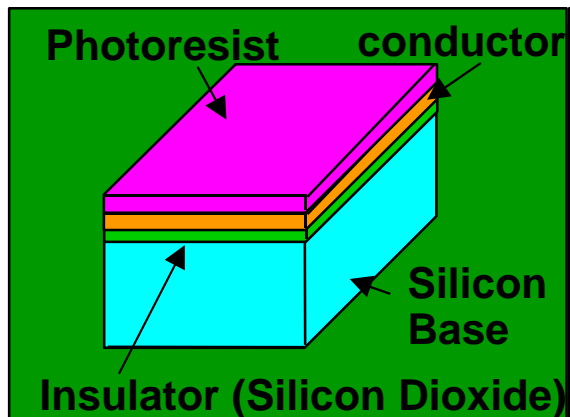
# Major steps in chip fabrication (cont.)

[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

**Step 3** - Silicon Ingots are grown in special furnaces called pullers.

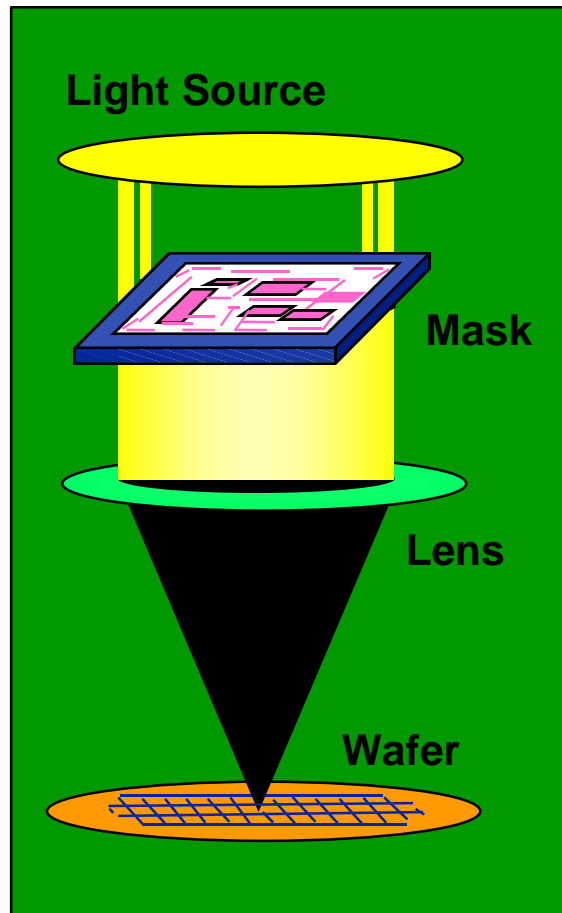
**Step 4** - Wafers are sliced off and polished.

**Step 5** - Flats are added for orientation.



**Step 6** - Layers are grown on the wafer in special diffusion furnaces.

# Major steps in chip fabrication (cont.)

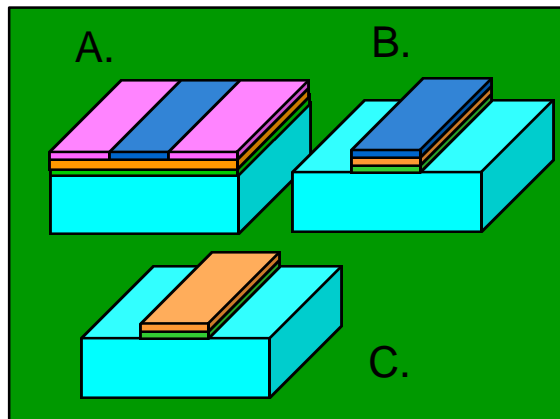
[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

**Step 7 - Photolithography** - A pattern or mask of the chip is made. Ultraviolet light projects the pattern repeatedly on the wafer. An image of the chip is transferred to the wafer in this process.

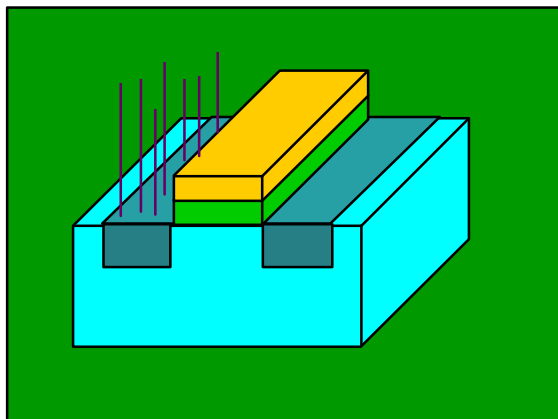


Stepper

# Major steps in chip fabrication (cont.)

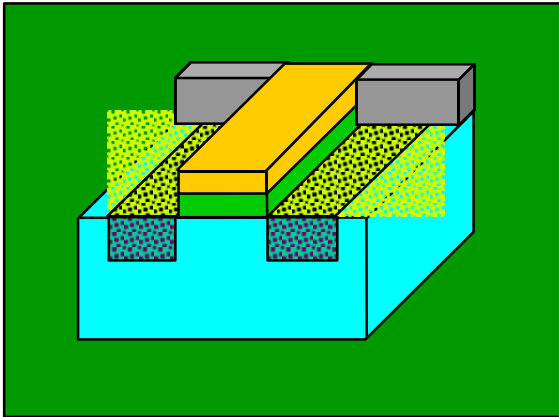
[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

**Step 8 - Etching** - Unwanted layers are etched away with gases or solvents. The hardened photoresist protects the underneath layers in figure B. Then the hardened photoresist is also etched away in figure C.

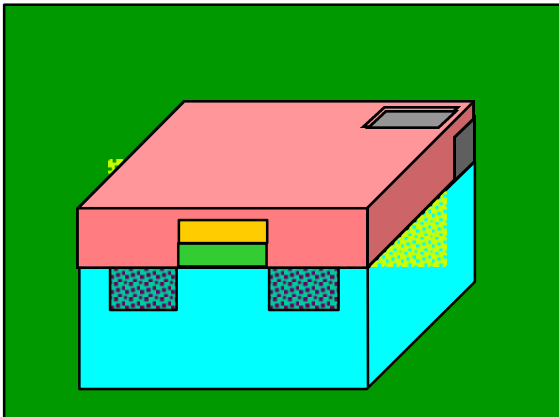


**Step 9 - Doping** - Positively charged dopant atoms are shot into the silicon base during an ion implantation process.

# Major steps in chip fabrication

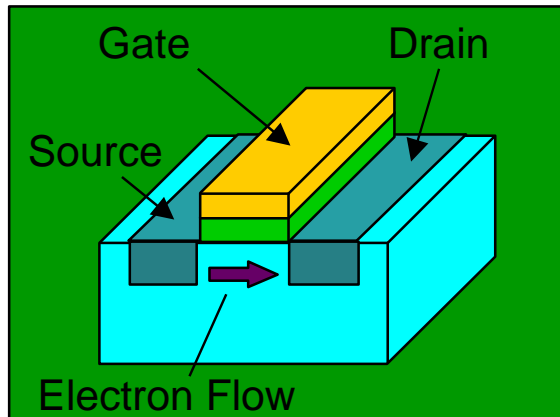
[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

**Step 10** - Deposition - individual devices are interconnected using a series of metal depositions.

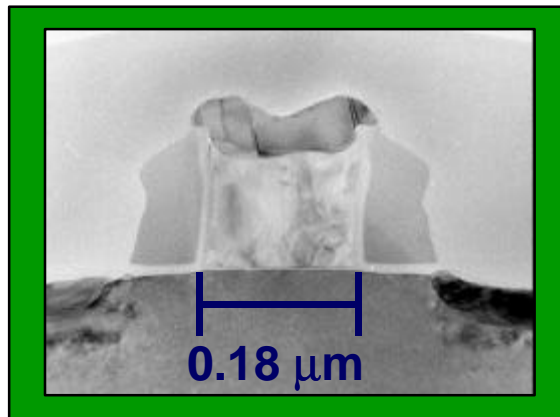


**Step 11** - Passivation - A final dielectric layer is deposited to protect the circuit from damage and contamination.

# Basics of chip operation

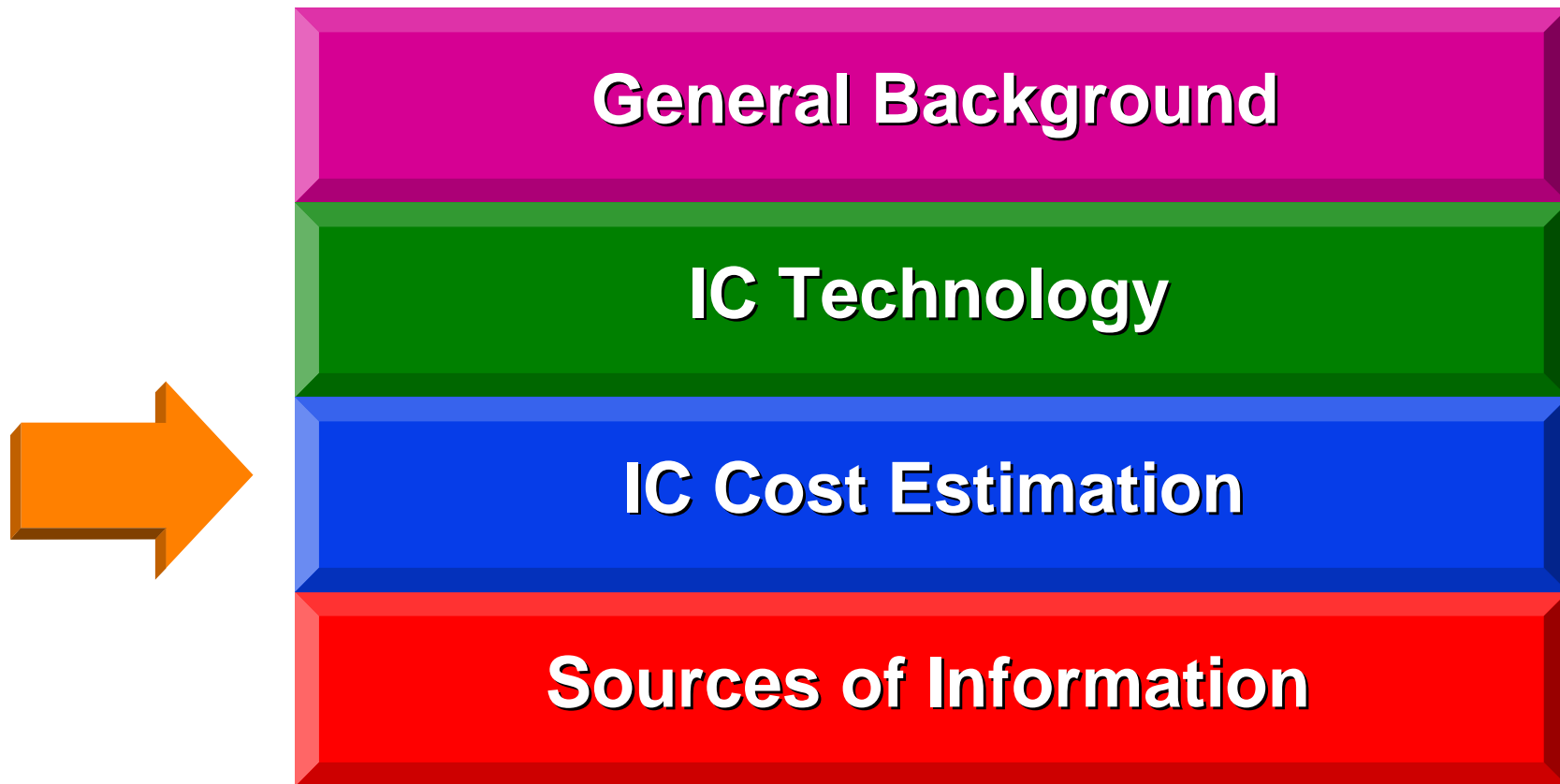
[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

**Operation** - When a positive voltage is applied to a gate, electrons move from the source to the drain. This switches the transistor on.



Photograph of a 0.18m gate using a scanning electron microscope.

# Detailed Cost Estimates



# The big three factors that drive IC cost



Background

IC Technology

IC Costing

Information

- 0 **Manufacturing Yield**

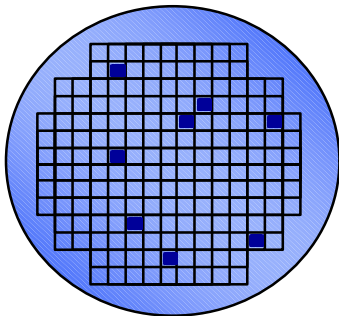
- 0 **Wafer Size**

- 0 **Factory Cost**

# Manufacturing Yield

[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

**Yield** = Number of good chips/Number of chips made

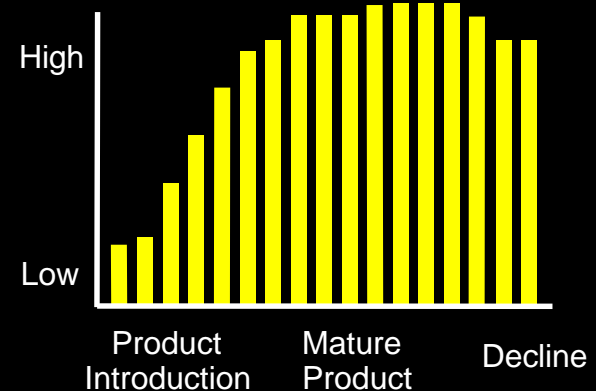


IC	DC Yield	Visual Yield	Wafer Yield	Total Yield
Chip 1	85%	75%	95%	61%
Chip 2	95%	90%	95%	81%

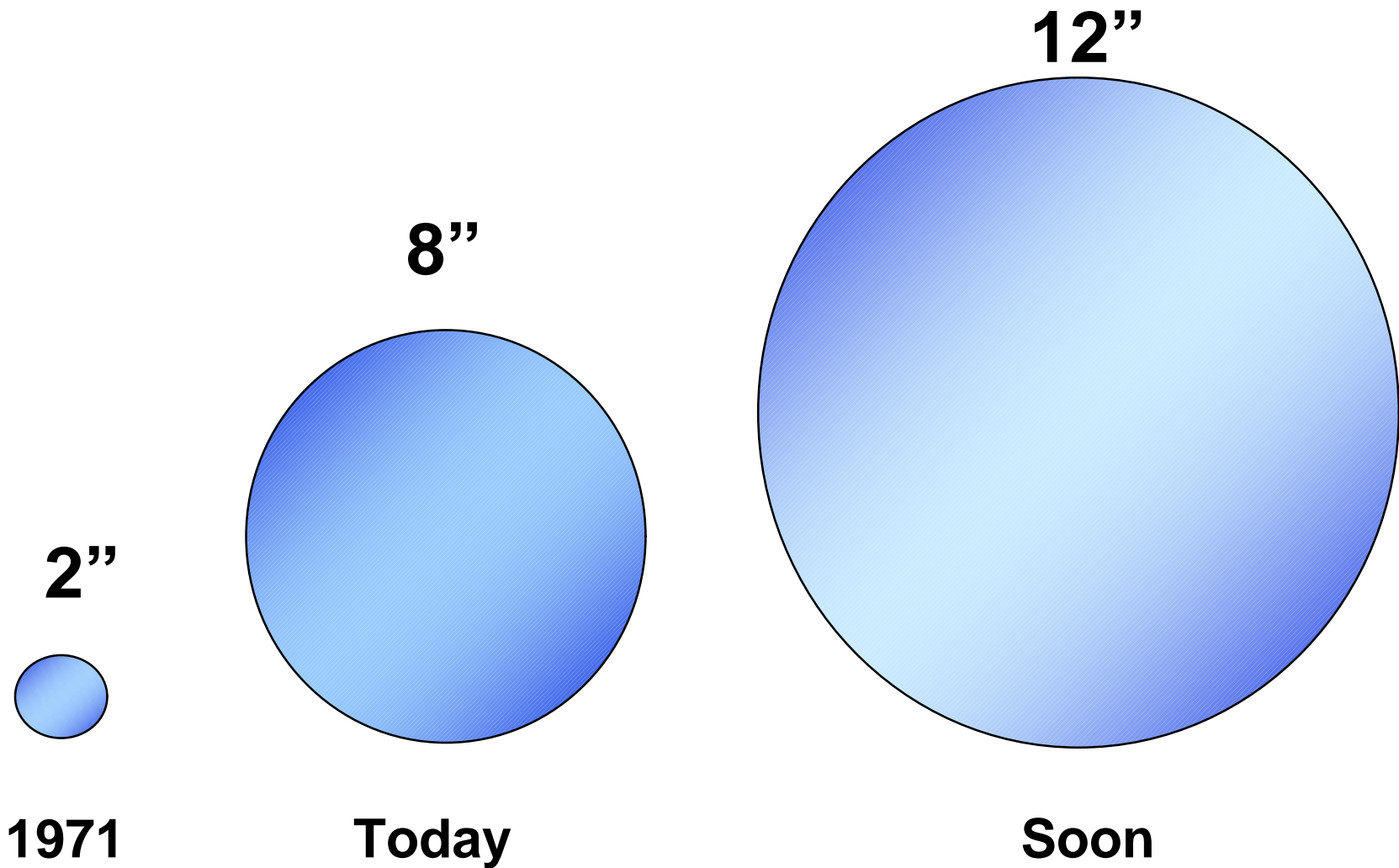
## Major Factors that influence Yield

- Feature Size
- Technology Type
- Number of gates or transistors
- Wafer Type
- Number of Process steps
- Point in product life cycle

## Yield vs. Time



# Larger wafer areas result in lower IC costs

[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

Source: Intel

# High Cost of an IC Factory

[Background](#)[IC Technology](#)[IC Costing](#)[Information](#)

- o **A High-End Semiconductor Foundry costs \$1.5 to \$3.0B**
  - **70% of the cost is found in the processing equipment.**
  - **An average plant has 30 to 40 different types of machines.**
  - **Currently, about 25 foundries are built per year.**
  - **Increasingly companies are teaming up to jointly build these facilities in order to share the cost.**



# Foundry utilization is critical to cost



Background

IC Technology

IC Costing

Information

$$\text{Foundry Utilization} = \frac{\text{Wafers Processed per month}}{\text{Foundry capacity (3 shifts)}}$$

- 0 Increased foundry utilization lowers the overhead and capital amortization costs assigned to each chip.
- 0 Low foundry loading (<20%) can provide a 3x increase in cost over a highly loaded foundry (>80%) -- TI study.
- 0 Low foundry utilization will show up via increased IC processing cost (\$/mm<sup>2</sup>).

# 3 Methods for IC Costing



Background

IC Technology

IC Costing

Information

- o **Analogy** - Use when lacking detailed information.
- o **Parametric Model** - Use when detailed information is available. Good for IC design estimates.
- o **Build-up** - Use when very detailed information such as yield, chip area and processing costs is available.

# Parametric model example: Price M

Background

IC Technology

IC Costing

Information

**PRICE Microcircuit\* - Estimates development and production costs.**

## Selected PRICE M Inputs:

IC Quantity	Number of New Cells
IC Length & Width	CAD Factor
Number of Pins	Design Iterations
Number of Gates	Wafer Size
Number of Transistors	Feature Size

\* PRICE M is a product of PRICE Systems, Lockheed Martin (1-800-43-PRICE)

# Build-up: sample calculation

Background

IC Technology

IC Costing

Information

Table 1. Number of chips

Chip	Technology	Feature Size (in $\mu\text{m}$ )	Number of chips per board	Number of boards	Total Number of chips
ASIC #1	CMOS	0.35	8	150	1,200
ASIC #2	CMOS	0.25	15	200	3,000
ASIC #3	CMOS	0.25	10	200	2,000

Table 2. Wafer geometry

Chip	Chip Area ( $\text{mm}^2$ )	Wafer Area ( $\text{mm}^2$ )	Wafer Useability factor	Useable Wafer Area ( $\text{mm}^2$ )	Number of chips per Wafer
ASIC #1	125	31,416	85%	26,704	214
ASIC #2	175	31,416	80%	25,133	144
ASIC #3	225	31,416	80%	25,133	112

# Build-up: sample calculation



Background

IC Technology

IC Costing

Information

Table 3. Yield impact

Chip	DC Yield	Visual Inspect Yield	Line Yield	Total Yield	No. of good chips per Wafer	Number of Wafers
ASIC #1	85%	95%	95%	77%	164	7.3
ASIC #2	80%	85%	90%	61%	88	34.1
ASIC #3	78%	83%	90%	58%	65	30.7

Table 4. Cost

Chip	Total Number of chips	Wafer Cost per (mm <sup>2</sup> )	Total Cost per Wafer	Cost per Good Chip	Total Cost All Chips
ASIC #1	1,200	\$0.25	\$7,854	\$47.93	\$57,510
ASIC #2	3,000	\$0.50	\$15,708	\$178.72	\$536,152
ASIC #3	2,000	\$0.55	\$17,279	\$265.49	\$530,970
TOTAL	6,200				\$1,124,632

# Wafer size and area conversion table

Background

IC Technology

IC Costing

Information

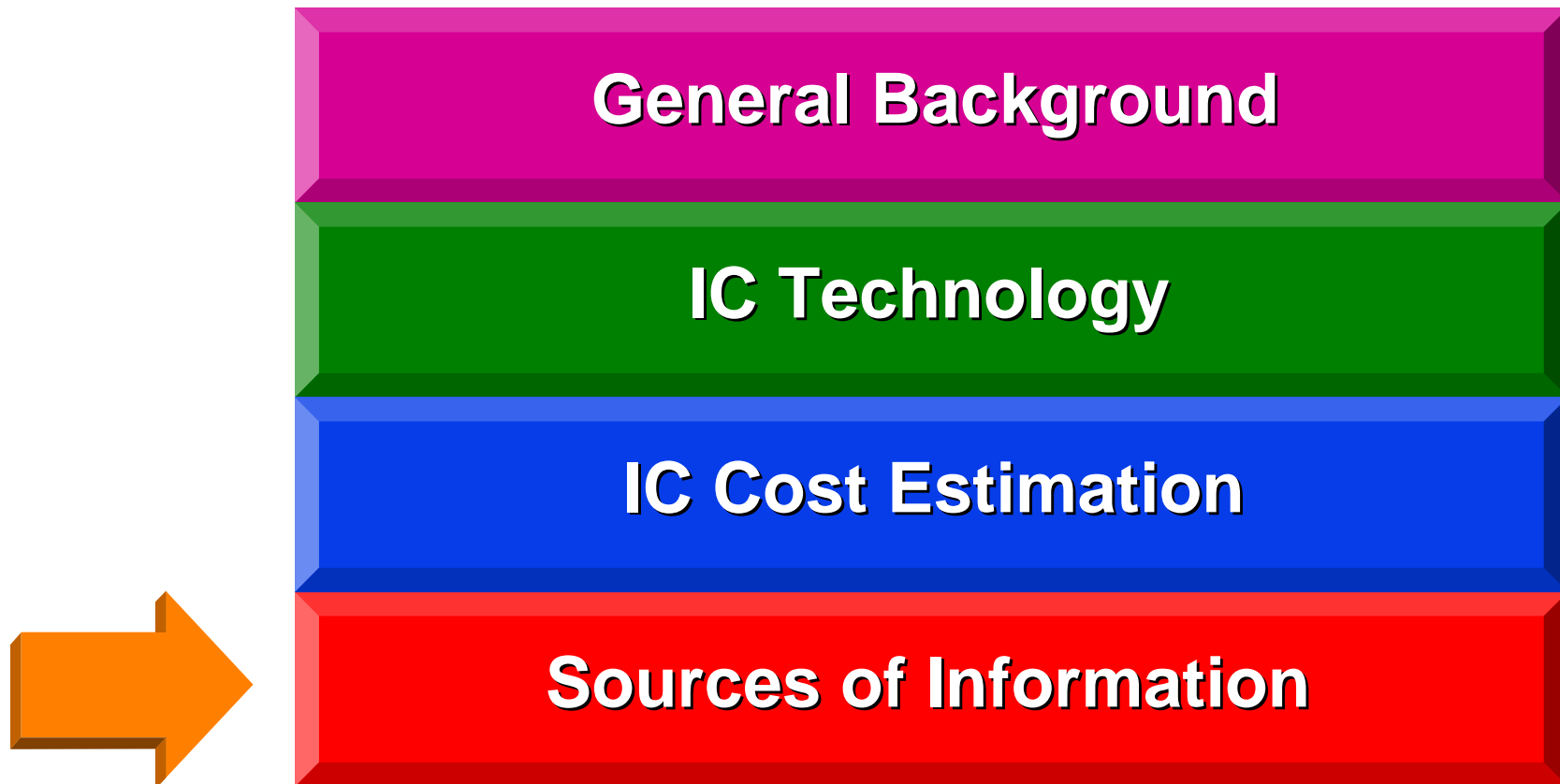
Wafer Size		Wafer Area*	
Inches	mm	In <sup>2</sup>	mm <sup>2</sup>
2.00	50.8	3.14	2,026
3.00	76.2	7.07	4,561
3.94	100.0	12.19	7,865
4.92	125.0	19.02	12,272
5.90	150.0	27.39	17,671
7.87	200.0	48.69	31,416
11.87	300.0	109.39	70,650

← GaAs

← Silicon

\* Note: Useable Area is normally between 70 to 90% of total area due to round edges, flats and test chips.

# Detailed Cost Estimates



# Additional sources of information

Background

IC Technology

IC Costing

Information

## Web Pages

Semiconductor Subway	<a href="http://www.goesser.mit.edu/semisubway">www.goesser.mit.edu/semisubway</a>
Semiconductor Industry Association	<a href="http://www.semichips.org">www.semichips.org</a>
Semiconductor Equipment and Materials International (SEMI)	<a href="http://www.semi.org">www.semi.org</a>
Semiconductor Online	<a href="http://www.semicondutoronline.com">www.semicondutoronline.com</a>
Semiconductor References	<a href="http://www.n-ablegroup.com/Database/ref">www.n-ablegroup.com/Database/ref</a>

## Books

Microchip Fabrication, Peter Van Zant  
McGraw-Hill, NY, 1997  
1-800-262-4729

Integrated Circuit Fabrication, David Elliott,  
McGraw-Hill, NY, 1982

## Journals

Solid State Technology, PennWell  
(603) 891-0123, [www.solid-state.com](http://www.solid-state.com)

IEEE Journal of Semiconductor  
Manufacturing